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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/645,782	08/22/2003	Keiichiro Kata	069974-0143	8077
22428	7590 01/19/2006		EXAMINER	
FOLEY AND LARDNER LLP			PRENTY, MARK V	
SUITE 500 3000 K STR	EET NW		ART UNIT	PAPER NUMBER
WASHINGT	WASHINGTON, DC 20007			
			DATE MAILED: 01/19/2000	5

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)	$\overline{}$	
		10/645,782	KATA ET AL.		
Office Action Summary		Examiner	Art Unit		
		MARK PRENTY	2822		
Period 1	The MAILING DATE of this communication ap for Reply	pears on the cover sheet w	th the correspondence addre	ss	
WHI - Ext afto - If N - Fai An	HORTENED STATUTORY PERIOD FOR REPLICHEVER IS LONGER, FROM THE MAILING Densions of time may be available under the provisions of 37 CFR 1. From the mailing date of this communication. O period for reply is specified above, the maximum statutory period lure to reply within the set or extended period for reply will, by statuty reply received by the Office later than three months after the mailing ned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNION (136(a)). In no event, however, may a rewill apply and will expire SIX (6) MON e, cause the application to become AE	CATION.  eply be timely filed  ITHS from the mailing date of this comm  BANDONED (35 U.S.C. § 133).		
Status					
1)[\	Responsive to communication(s) filed on 28 L	<u>December 2005</u> .			
2a)[	This action is <b>FINAL</b> . 2b) This action is non-final.				
3)	Since this application is in condition for allowa	ance except for formal matt	ers, prosecution as to the ma	erits is	
	closed in accordance with the practice under	Ex parte Quayle, 1935 C.D	). 11, 453 O.G. 213.		
Disposi	tion of Claims				
4)[🗆	Claim(s) 1-12,15,16 and 25-32 is/are pending	in the application.			
	4a) Of the above claim(s) is/are withdra	awn from consideration.			
5)[🗆	Claim(s) <u>3-12,15,16,27,28,31 and 32</u> is/are all	lowed.			
·	Claim(s) <u>1 and 2</u> is/are rejected.				
7)⊠					
8)∐	Claim(s) are subject to restriction and/o	or election requirement.			
Applica	tion Papers				
9)[	The specification is objected to by the Examine	er.			
10)	The drawing(s) filed on is/are: a) acc	cepted or b) objected to	by the Examiner.		
	Applicant may not request that any objection to the	drawing(s) be held in abeyar	ice. See 37 CFR 1.85(a).		
	Replacement drawing sheet(s) including the correct	,	• •		
11)∟	The oath or declaration is objected to by the E	xaminer. Note the attached	I Office Action or form PTO-	152.	
Priority	under 35 U.S.C. § 119				
•	Acknowledgment is made of a claim for foreigr )□ All b)□ Some * c)□ None of:	n priority under 35 U.S.C. §	119(a)-(d) or (f).		
	1. Certified copies of the priority document				
	2. Certified copies of the priority document				
	3. Copies of the certified copies of the price	-	received in this National Sta	ige	
*	application from the International Burea See the attached detailed Office action for a list		rocaived		
	See the attached detailed Office action for a list	to the certified copies flot	received.		
Attachme	• •	_			
	ice of References Cited (PTO-892)		Summary (PTO-413) s)/Mail Date.		
	ice of Draftsperson's Patent Drawing Review (PTO-948) rmation Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	_ ' '	s/Mail Date. <u>20000773</u> nformal Patent Application (PTO-15	2)	
	er No(s)/Mail Date	6) Other:	<b>-</b> ∙		

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This Office Action is in response to the full and proper response filed on

December 28, 2005, which has been entered in its entirety. The Advisory Action mailed

on January 10, 2006, is withdrawn.

Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by

United States Patent 5,327,013 to Moore et al. (Moore).

As to independent claim 1, Moore discloses a semiconductor wafer (see the

entire patent, particularly the Figs. 1-2 disclosure), including: a plurality of [chip]

sections 10 defined thereon by scribe lines (see column 2, lines 45-47), each chip

section 10 having bump electrodes 30 formed simultaneously thereon (see column 2,

lines 45-52), the scribe lines for separating the chip sections from each other without

dividing bump electrodes thereon, said chip section 10 including: a plurality of chip

electrodes 16 positioned on said chip section (see column 2, lines 31-36); and a

plurality of interconnection layers 26/24 for electrically connecting said chip electrodes

16 and said bump electrodes 30, said bump electrodes 30 being located at positions

other than over said chip electrodes 16, said chip section having a center and a

periphery 18 and said interconnection layers 26/24 extend from said periphery toward

said center.

Claim 1 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Moore.

As to independent claim 2, Moore discloses a semiconductor wafer (see the

entire patent, particularly the Figs. 1-2 disclosure), including: a plurality of [chip]

sections 10 defined thereon by scribe lines (see column 2, lines 45-47), each chip

section 10 having: bump electrodes 30 formed simultaneously thereon (see column 2,

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lines 45-52); a plurality of chip electrodes 16 positioned on said chip section (see

column 2, lines 31-36); and a plurality of interconnection layers 26/24 for electrically

connecting said chip electrodes 16 and said bump electrodes 30, said bump electrodes

30 being located at positions other than over said chip electrodes 16, said chip section

having a center and a periphery 18 and said interconnection layers 26/24 extend from

said periphery toward said center.

Claim 2 is thus rejected under 35 U.S.C. 102(b) as being anticipated by Moore.

Claims 25, 26, 29 and 30 are objected to as being dependent upon a rejected

base claim, but would be allowable over the prior art of record if rewritten in

independent form including all of the limitations of the base claim and any intervening

claims.

Claims 3-12, 15, 16, 27, 28, 31 and 32 are allowable over the prior art of record.

The prior art of record does not disclose or suggest the allowable semiconductor

wafers taken as a whole, including the interconnection layers.

Registered practitioners can telephone the examiner at (571) 272-1843. Any

voicemail message left for the examiner must include the name and registration number

of the registered practitioner calling, and the Application/Control (Serial) Number.

Technology Center 2800's general telephone number is (571) 272-2800.

Mark V. Prenty

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